

# Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

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## The MOSFET – Metal Oxide FET

In contrast to the Junction Field Effect Transistor (JFET), the Insulated Gate Field Effect Transistor (IGFET) has its Gate input electrically insulated from the main current carrying channel. The most common type of insulated gate FET which is used in many different types of electronic circuits is called the Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

The IGFET or MOSFET is a voltage controlled field effect transistor that differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass. This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the MOSFET extremely high way up in the Mega-ohms ( $M\Omega$ ) region thereby making it almost infinite. As the Gate terminal is isolated from the main current carrying channel “NO current flows into the gate” and just like the JFET, the MOSFET also acts like a voltage controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the MOSFET becoming easily damaged unless carefully handled or protected.

Like the previous JFET tutorial, MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

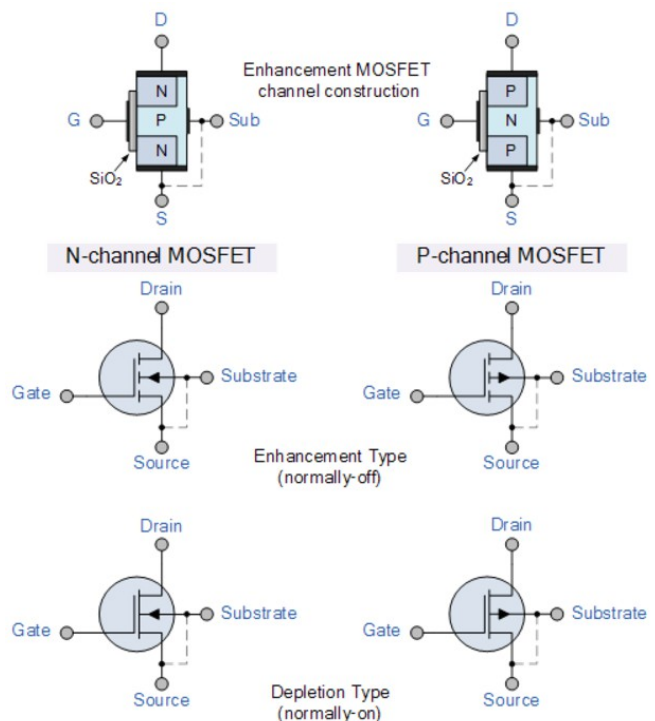
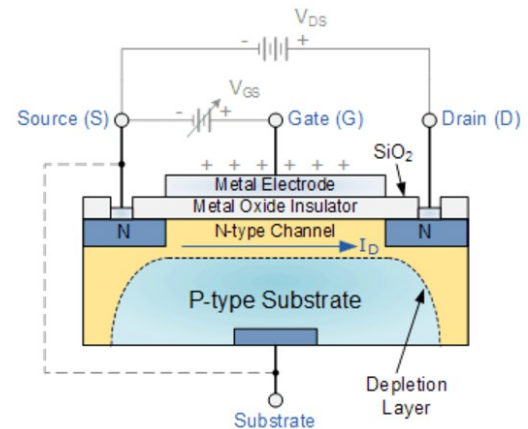
**Depletion Type** – the transistor requires the Gate-Source voltage, ( $V_{GS}$ ) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “Normally Closed” switch.

**Enhancement Type** – the transistor requires a Gate-Source voltage, ( $V_{GS}$ ) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “Normally Open” switch.

The symbols and basic construction for both configurations of MOSFETs are shown on the right.

The four MOSFET symbols on the right show an additional terminal called the Substrate and is not normally used as either an input or an output connection but instead it is used for grounding the substrate. It connects to the main semiconductive channel through a diode junction to the body or metal tab of the MOSFET. Usually in discrete type MOSFETs, this substrate lead is connected internally to the source terminal. When this is the case, as in enhancement types it is omitted from the symbol for clarification.

The line between the drain and source connections represents the semiconductive channel. If this is a solid unbroken line then this represents a “Depletion” (normally-ON) type MOSFET as drain current can flow



with zero gate potential. If the channel line is shown dotted or broken it is an “Enhancement” (normally-OFF) type MOSFET as zero drain current flows with zero gate potential. The direction of the arrow indicates whether the conductive channel is a p-type or an n-type semiconductor device.

Referring to the first figure on the previous page, the construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semiconductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes.

For a junction field effect transistor (JFET), its gate must be biased in such a way as to reverse-bias the pn-junction. With an insulated gate MOSFET device no such limitations apply so it is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve). This makes the MOSFET device especially valuable as electronic switches or to make logic gates because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the p-channel and the n-channel MOSFETs are available in two basic forms, the Enhancement type and the Depletion type.

### Depletion-mode MOSFET

The Depletion-mode MOSFET, which is less common than the enhancement mode types is normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when  $V_{GS} = 0$  making it a “normally-closed” device. The circuit symbol shown above for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel.

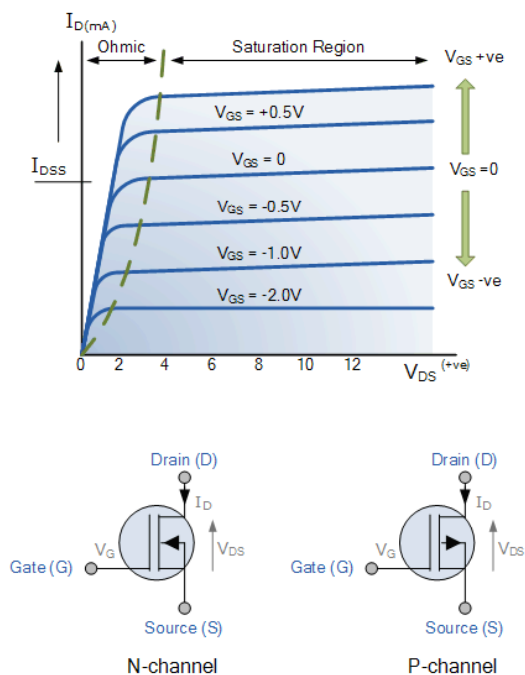
For the n-channel depletion MOS transistor, a negative gate-source voltage,  $-V_{GS}$  will deplete (hence its name) the conductive channel of its free electrons switching the transistor “OFF”. Likewise for a p-channel depletion MOS transistor a positive gate-source voltage,  $+V_{GS}$  will deplete the channel of its free holes turning it “OFF”.

In other words, for an n-channel depletion mode MOSFET:  $+V_{GS}$  means more electrons and more current. While a  $-V_{GS}$  means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a “normally-closed” switch.

The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts were the drain-source channel is inherently conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the Drain and Source with zero Gate bias.

### Enhancement-mode MOSFET

The more common Enhancement-mode MOSFET or eMOSFET, is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally “OFF” (non-conducting) when the gate bias voltage,  $V_{GS}$  is equal to zero. The circuit symbol shown above for an enhancement MOS transistor uses a broken channel line to signify a normally open non-conducting channel.



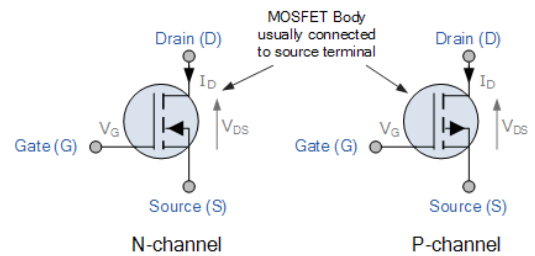
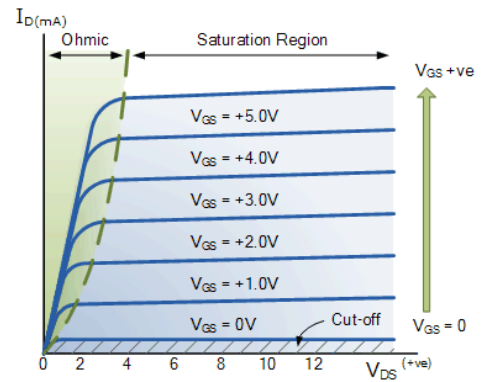
For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage ( $V_{GS}$ ) is applied to the gate terminal greater than the threshold voltage ( $V_{TH}$ ) level in which conductance takes place making it a transconductance device.

The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.

Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current,  $I_D$  through the channel. In other words, for an n-channel enhancement mode MOSFET:  $+V_{GS}$  turns the transistor “ON”, while a zero or  $-V_{GS}$  turns the transistor “OFF”. Then, the enhancement-mode MOSFET is equivalent to a “normally-open” switch.

The reverse is true for the p-channel enhancement MOS transistor. When  $V_{GS} = 0$  the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET:  $+V_{GS}$  turns the transistor “OFF”, while  $-V_{GS}$  turns the transistor “ON”.

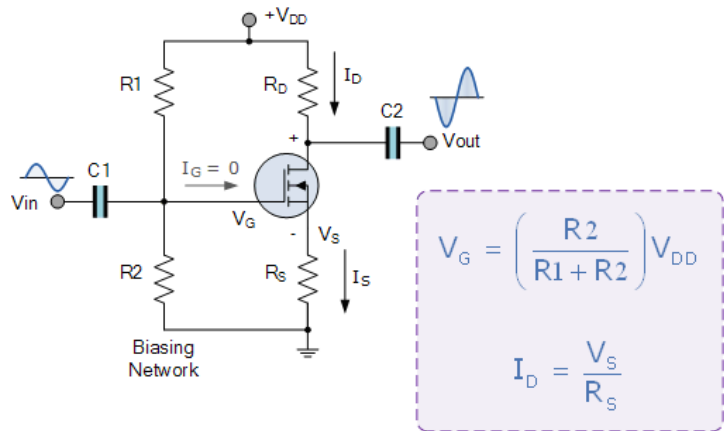
Enhancement-mode MOSFETs make excellent electronics switches due to their low “ON” resistance and extremely high “OFF” resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type Logic Gates and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for Complementary MOS meaning that the logic device has both PMOS and NMOS within its design.



### The MOSFET Amplifier

Just like the previous Junction Field Effect transistor, MOSFETs can be used to make single stage class “A” amplifier circuits with the enhancement mode n-channel MOSFET common source amplifier being the most popular circuit. The depletion mode MOSFET amplifiers are very similar to the JFET amplifiers, except that the MOSFET has a much higher input impedance.

This high input impedance is controlled by the gate biasing resistive network formed by  $R_1$  and  $R_2$ . Also, the output signal for the enhancement mode common source MOSFET amplifier is inverted because when  $V_G$  is low the transistor is switched “OFF” and  $V_D$  ( $V_{out}$ ) is high. When  $V_G$  is high the transistor is switched “ON” and  $V_D$  ( $V_{out}$ ) is low as shown.



The DC biasing of this common source (CS) MOSFET amplifier circuit is virtually identical to the JFET amplifier. The MOSFET circuit is biased in class A mode by the voltage divider network formed by resistors  $R_1$

and R2. The AC input resistance is given as  $R_{IN} = R_G = 1M\Omega$ .

Metal Oxide Semiconductor Field Effect Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The MOSFETs ability to change between these two states enables it to have two basic functions: “switching” (digital electronics) or “amplification” (analogue electronics). Then MOSFETs have the ability to operate within three different regions:

1. Cut-off Region – with  $V_{GS} < V_{TH}$  the gate-source voltage is lower than the threshold voltage so the MOSFET transistor is switched “fully-OFF” and  $I_{DS} = 0$ , the transistor acts as an open circuit.
2. Linear (Ohmic) Region – with  $V_{GS} > V_{TH}$  and  $V_{DS} < V_{GS}$  the transistor is in its constant resistance region and behaves as a voltage-controlled resistor whose resistive value is determined by the gate voltage,  $V_{GS}$ .
3. Saturation Region – with  $V_{GS} > V_{TH}$  the transistor is in its constant current region and is switched “fully-ON”. The current  $I_{DS} = \text{maximum}$  as the transistor acts as a closed circuit.

### MOSFET Summary

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has an extremely high input gate resistance with the current flowing through the channel between the source and drain being controlled by the gate voltage. Because of this high input impedance and gain, MOSFETs can be easily damaged by static electricity if not carefully protected or handled. MOSFET’s are ideal for use as electronic switches or as common-source amplifiers as their power consumption is very small. Typical applications for MOSFET's are in microprocessors, memories, calculators, and logic CMOS gates, etc.

Also, notice that a dotted or broken line within the symbol indicates a normally “OFF” enhancement type showing that “NO” current can flow through the channel when zero gate-source voltage  $V_{GS}$  is applied. A continuous unbroken line within the symbol indicates a normally “ON” Depletion type showing that current “CAN” flow through the channel with zero gate voltage. For p-channel types the symbols are exactly the same for both types except that the arrow points outwards. This can be summarized in the following switching table.

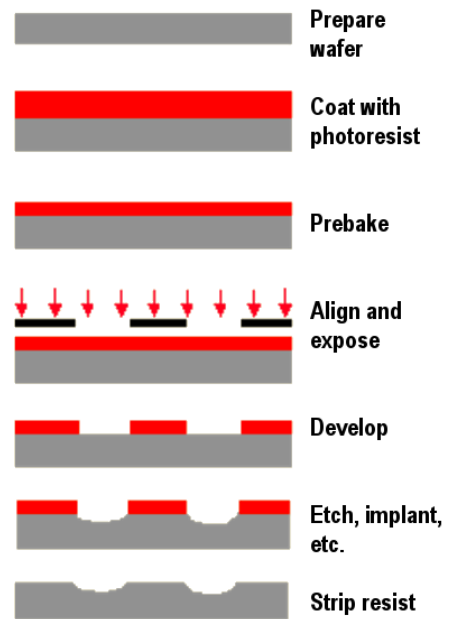
MOSFET type	$V_{GS} = +ve$	$V_{GS} = 0$	$V_{GS} = -ve$
N-Channel Depletion	ON	ON	OFF
N-Channel Enhancement	ON	OFF	OFF
P-Channel Depletion	OFF	ON	ON
P-Channel Enhancement	OFF	OFF	ON

So for n-type enhancement type MOSFETs, a positive gate voltage turns “ON” the transistor and with zero gate voltage, the transistor will be “OFF”. For a p-channel enhancement type MOSFET, a negative gate voltage will turn “ON” the transistor and with zero gate voltage, the transistor will be “OFF”. The voltage point at which the MOSFET starts to pass current through the channel is determined by the threshold voltage  $V_{TH}$  of the device.

# Semiconductor Lithography (Photolithography)

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The fabrication of an integrated circuit (IC) requires a variety of physical and chemical processes performed on a semiconductor (e.g., silicon) substrate. In general, the various processes used to make an IC fall into three categories: film deposition, patterning, and semiconductor doping. Films of both conductors (such as polysilicon, aluminum, and more recently copper) and insulators (various forms of silicon dioxide, silicon nitride, and others) are used to connect and isolate transistors and their components. Selective doping of various regions of silicon allow the conductivity of the silicon to be changed with the application of voltage. By creating structures of these various components millions of transistors can be built and wired together to form the complex circuitry of a modern microelectronic device. Fundamental to all of these processes is lithography, i.e., the formation of three-dimensional relief images on the substrate for subsequent transfer of the pattern to the substrate.



The word lithography comes from the Greek lithos, meaning stones, and graphia, meaning to write. It means quite literally writing on stones. In the case of semiconductor lithography (also called photolithography) our stones are silicon wafers and our patterns are written with a light sensitive polymer called a photoresist. To build the complex structures that make up a transistor and the many wires that connect the millions of transistors of a circuit, lithography and etch pattern transfer steps are repeated at least 10 times, but more typically are done 20 to 30 times to make one circuit. Each pattern being printed on the wafer is aligned to the previously formed patterns and slowly the conductors, insulators, and selectively doped regions are built up to form the final device.

The importance of lithography can be appreciated in two ways. First, due to the large number of lithography steps needed in IC manufacturing, lithography typically accounts for about 30 percent of the cost of manufacturing. Second, lithography tends to be the technical limiter for further advances in feature size reduction and thus transistor speed and silicon area. Obviously, one must carefully understand the trade-offs between cost and capability when developing a lithography process. Although lithography is certainly not the only technically important and challenging process in the IC manufacturing flow, historically, advances in lithography have gated advances in IC cost and performance.

Optical lithography is basically a photographic process by which a light sensitive polymer, called a photoresist, is exposed and developed to form three-dimensional relief images on the substrate. In general, the ideal photoresist image has the exact shape of the designed or intended pattern in the plane of the substrate, with vertical walls through the thickness of the resist. Thus, the final resist pattern is binary: parts of the substrate are covered with resist while other parts are completely uncovered. This binary pattern is needed for pattern transfer since the parts of the substrate covered with resist will be protected from etching, ion implantation, or other pattern transfer mechanism.

The general sequence of processing steps for a typical photolithography process is as follows: substrate preparation, photoresist spin coat, prebake, exposure, post-exposure bake, development, and postbake. A resist strip is the final operation in the lithographic process, after the resist pattern has been transferred into the underlying layer. This sequence is shown diagrammatically in Figure 1-1, and is generally performed on several tools linked together into a contiguous unit called a lithographic cluster. A brief discussion of each step is given below, pointing out some of the practical issues involved in photoresist processing.

# Progression of Node Size Shrink Since 1970

Wikipedia

The *technology node* (also *process node*, *process technology* or simply *node*) is traditionally defined as the smallest half-pitch of contacted metal 1 lines (lowest level metal in the process) allowed in the fabrication process. It is a common metric used to describe and differentiate the technologies used in fabricating integrated circuits. The state-of-the-art technology (2017) for mass production of IC chips is with a node size of 10 nm. It is projected that the node size will be reduced to 5 nm in 2020. Next-generation lithography (NGL) is a term used in integrated circuit manufacturing to describe the lithography technologies slated to replace photolithography. As of 2016 the most advanced form of photolithography is immersion lithography, in which water is used as an immersion medium for the final lens. It is being applied to the 16 nm and 14 nm nodes, with the required use of multiple patterning. The increasing costs of multiple patterning have motivated the continued search for a next-generation technology that can flexibly achieve the required resolution in a single processing step. Candidates for next-generation lithography include: extreme ultraviolet lithography (EUV-lithography), X-ray lithography, electron beam lithography, focused ion beam lithography, and nanoimprint lithography. Electron beam lithography was most popular during the 1970s, but was replaced in popularity by X-ray lithography during the 1980s and early 1990s, and then by EUV lithography from the mid-1990s to the mid-2000s. Focused ion beam lithography has carved a niche for itself in the area of defect repair. Nanoimprint's popularity is rising, and is positioned to succeed EUV as the most popular choice for next-generation lithography, due to its inherent simplicity and low cost of operation as well as its success in the LED, hard disk drive and microfluidics sectors.

